WHAT IS CLAIMED IS:

1. A bus agent comprising:

a plurality of request and address interfaces for a plurality of request and address signals;

a target ready interface for a target ready signal;

a data bus busy interface for a data bus busy signal;

a plurality of response interfaces for a plurality of response signals;

a bus controller to track a plurality of transactions comprising a transaction N-1 and a transaction N, the bus controller being capable of asserting the target ready signal for transaction N if the bus agent is asserting the data bus busy signal for the transaction N-1 and deasserts the data bus busy signal.

2. The bus agent of claim 1 wherein said bus controller is to track a plurality of a phases of a plurality of bus transactions, said bus controller to track a transaction P-1 and a transaction P, wherein said bus controller is capable of asserting a response for transaction P two or more bus clock cycles after asserting a response for transaction P-1.

3. The bus agent of claim 1 further comprising:

a control interface to drive a control signal at the bus clock frequency;

an address bus interface to drive address elements at twice the bus clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to drive data elements at four times the bus clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element.

4. The bus agent of claim 3 wherein said address bus interface is to drive a first address strobe at the bus clock frequency, said first address strobe having a first address strobe transition of a first polarity to be substantially centered on a first address element and a second address strobe transition of a second polarity to be substantially centered on a second address element, the second address element being consecutive to the first address element, and wherein said data bus interface is to drive four consecutive data elements and a first data strobe and a second data strobe, and wherein a first edge of a first polarity of the first data strobe is to be substantially centered on a first data element, a first edge of the first polarity of the second data strobe is to be substantially centered on a second data element, a second edge of the first polarity of the first data strobe is to be substantially centered on a third data element, and a second edge of the first polarity of the second data strobe is to be substantially centered on a fourth data element.

5. The bus agent of claim 3 wherein said data bus interface is to generate first, second, third, and fourth data elements in a first signal generation time period and wherein said address bus interface is to generate first and second address elements in a second signal generation time period, said first signal generation time period and said second signal generation time period each being substantially equivalent to a clock cycle of the bus clock signal, wherein:

a first edge of a first data strobe is to be positioned at approximately a 12.5 percent point of the first signal generation time period;

a first edge of a second data strobe is to be positioned at approximately a 37.5 percent point of said first signal generation time period;

a second edge of said first data strobe is to be positioned at approximately a 67.5 percent point of the first signal generation time period;

a second edge of said second data strobe is to be positioned at approximately a 87.5 percent point of the first signal generation time period;

said first data element to be generated at approximately a beginning of the first signal generation time period;

said second data element is to be transmitted at approximately a twenty five percent point of the first signal generation time period;

said third data element is to be transmitted at approximately a fifty percent point of the first signal generation time period;

said fourth data element is to be transmitted at approximately a seventy five percent point of the first signal generation time period.

a first edge of a first address strobe is to be positioned at approximately a twenty five percent of said second signal generation time period,

a second edge of said first address strobe is to be positioned at approximately a seventy five percent of said second signal generation time period;

said first address elements is to be transmitted at approximately a beginning of the second signal generation time period;

said second address elements is to be transmitted at approximately a fifty percent point of the second signal generation time period.

6. The bus agent of claim 3 further comprising:

address strobe generation logic to generate a first address strobe to have a first address strobe transition at substantially a first address element center point of a first address element driving window in which a first address element is to be driven, and wherein

said address strobe generation logic is to generate said first address strobe to have a second transition at substantially a second address element center point of a second address element driving window in which a second address element is to be driven;

data strobe generation logic to generate a first data strobe to have a first transition of the first data strobe at substantially a first data element center point of a first data element driving window in which the a data element is to be driven, and wherein

said data strobe generation logic is to generate a second data strobe to have a first transition of the second data strobe at substantially a second data element center point of a second data element driving window in which the second data element is to be driven, and wherein

said data strobe generation logic is to generate a second transition of the first data strobe to have a second transition of the first data strobe at substantially a third data element center point of a third data element driving window in which a third data element is to be driven, and wherein

said data strobe generation logic is to generate a second transition of the second data strobe to have a second transition of the second data strobe at substantially a fourth data element center point of a fourth data element driving window in which the fourth data element is to be driven.

7. A method comprising:

asserting a data bus busy signal for an N-1th transaction in a first bus clock cycle;

asserting a target ready signal for an Nth transaction in a second bus clock cycle which is adjacent to said first bus clock cycle only if the data bus busy signal is deasserted in the second bus cycle and if a bus agent asserting the data bus

busy signal in the first bus clock cycle deasserts the data bus busy signal.

8. The method of claim 7 further comprising:

tracking a transaction P and a transaction P-1;

asserting a response for transaction P two bus clock cycles after asserting a response for transaction P-1.

9. The method of claim 7 further comprising:

generating a first address element and a second address element in a first duration substantially equivalent to a bus clock cycle of the bus clock signal

generating an address strobe having a first address strobe transition substantially centered on said first address element and having second address strobe transition substantially centered on said second address element;

generating a first data element, a second data element, a third data element, and a fourth data element in a second duration substantially equivalent in duration to the bus clock cycle of the bus clock signal;

generating a plurality of data strobe signals to provide a data strobe transition substantially centered on each data element.

10. The method of claim 9 further comprising:

generating a common clock address strobe control signal according to a common

clock protocol during a bus clock cycle in which transfer of said first and second address elements commences.

11. The method of claim 10 wherein said first address strobe transition has a first polarity and said second address strobe transition has a second polarity.

12. A system comprising:

a bus;

a processor to initiate a plurality of write transactions comprising a first write transaction and a second write transaction;

a chipset component to respond to said plurality of write transactions, said chipset to assert a target ready signal for the second write transaction in a next bus clock cycle if the chipset component asserts a data bus busy signal for the first write transaction in a previous bus clock cycle that is immediately previous to the next bus clock cycle and if the chipset component deasserts the data bus busy signal in the next bus clock cycle in which the target ready signal for the second write transaction is asserted.

13. The system of claim 12 wherein said processor is to initiate a transaction N-1 and a transaction N, and further wherein said chipset is to assert a response to transaction N two cycles after asserting a response to transaction N.

14. The system of claim 12 wherein said processor and said chipset component each further comprises:

a control interface to drive and receive a control signal at a clock frequency;

an address bus interface to drive and receive address elements at twice the clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element driven;

a data bus interface to drive and receive data elements at four times the clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element driven.

15. The system of claim 14 wherein said bus controller logic is capable of initiating an arbitration phase after two bus clock cycles from a prior arbitration phase and capable of receiving a block next request signal two bus clock cycles after assertion of an address strobe signal occurs and capable of responding to said block next request signal, and is capable of initiating a second request phase for a second transaction in a current cycle two bus clock cycles after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more bus clock cycles

prior to the current cycle.

16. A processor comprising:

logic to generate a full speed write line transaction by performing, in a plurality of consecutive bus clock cycles T1 through T16, the acts of:

asserting a first ADS# for a first transaction in T1, a second ADS# for a second transaction in T3, a third ADS# for a third transaction in T5, and a fourth ADS# for a fourth transaction in T7;

generating a first request in T1, a second request in T3, a third request in T5, and a fourth request in T7, respectively for the first through fourth transactions;

receiving a first TRDY# at the end of T3, a second TRDY# at the end of T7, a third TRDY# at the end of T9 through the end of T11, and a fourth TRDY# at the end of T13 through the end of T14;

asserting DBSY# in T5, T9, T11, and T15;

driving data in a source synchronous manner at a rate equivalent to four data elements per bus clock cycle in T5 through T6, T9 through T12, and T15 through T16; and

asserting DRDY# in T5 through T6, T9 through T12, and T15 through T16.

17. The processor of claim 16 further comprising logic to sample a plurality of cache status signals at the end of T4, T6, T8 and T10

18. A chipset comprising:

logic to respond to a full speed write line transaction by performing, in a plurality of consecutive bus clock cycles T1 through T16, the acts of:

receiving a first ADS# for a first transaction generated in T1, a second ADS# for a second transaction generated in T3, a third ADS# for a third transaction generated in T5, and a fourth ADS# for a fourth transaction generated in T7;

receiving a first request generated in T1, a second request generated in T3, a third request generated in T5, and a fourth request generated in T7, respectively for the first through fourth transactions;

generating a first TRDY# in T3, a second TRDY# in T7, a third TRDY# in T9 through T11, and a fourth TRDY# in T13 through T14;

receiving DBSY# asserted in T5, T9, T11, and T15;

receiving data in a source synchronous manner at a rate equivalent to four data elements per bus clock cycle driven in T5 through T6, T9 through T12, and T15 through T16; and

receiving DRDY driven in T5 through T6, T9 through T12, and T15 through T16.

19. A processor comprising:

logic to generate a read-write-write-read sequence of transactions by performing, in a plurality of consecutive bus clock cycles T1 through T16, the acts of:

asserting a first ADS# for a first read transaction in T1, a second ADS# for a first write transaction in T3, a third ADS# for a second write transaction in T5, and a fourth ADS# for a second read transaction in T7;

generating a first request in T1, a second request in T3, a third request in T5, and a fourth request in T7, respectively for the first read, first write, second write, and second read transactions;

receiving a first TRDY# at the end of T7, and a second TRDY# at the end of T9 through the end of T11;

asserting or sensing that DBSY# was asserted only in T6, T9, T11, and T14;

driving data in a source synchronous manner at a rate equivalent to four data elements per bus clock cycle in T6 through T7, T9 through T12, and T14 through T15.

20. A chipset comprising:

logic to respond to a read-write-write-read sequence of transactions by performing, in a plurality of consecutive bus clock cycles T1 through T16, the acts of:

receiving a first ADS# for a first read transaction in T1, a second ADS# for a first write transaction in T3, a third ADS# for a second write transaction in T5, and a fourth ADS# for a second read transaction in T7;

receiving a first request generated in T1, a second request generated in T3, a third request generated in T5, and a fourth request generated in T7, respectively for the first read, first write, second write, and second read transactions;

asserting TRDY# in T7 and deasserting TRDY# in T8;

asserting TRDY# in T9 and deasserting TRDY# in T12;

asserting or sensing that DBSY# was asserted only in T6, T9, T11, and T14;

driving data in a source synchronous manner at a rate equivalent to four data elements per bus clock cycle in T6 through T7, T9 through T12, and T14 through T15.

21. A bus agent comprising:

a plurality of response interfaces;

a clock interface to receive a bus clock signal operating at a bus clock frequency;

a bus controller to track a plurality of a phases of a plurality of bus transactions on a bus which is a multi-phase pipelined bus, said bus controller to track a transaction N-1 and a transaction N, wherein said bus controller is capable of

asserting a response for transaction N two or more bus clock cycles after asserting a response for transaction N-1;

a control interface to drive a control signal at the bus clock frequency;

an address bus interface to drive address elements at twice the bus clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to drive data elements at four times the bus clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element;

wherein said address bus interface is to drive a first address strobe at the bus clock frequency, said first address strobe having a first address strobe transition of a first polarity to be substantially centered on a first address element and a second address strobe transition of a second polarity to be substantially centered on a second address element, the second address element being consecutive to the first address element, and wherein said data bus interface is to drive four consecutive data elements and a first data strobe and a second data strobe, and wherein a first edge of a first polarity of the first data strobe is to be substantially centered on a first data element, a first edge of the first polarity of the second data strobe is to be substantially centered on the second data element, a second edge of the first polarity the first data strobe is to be substantially centered on the third data element, and a second edge of the first

polarity of the second data strobe is to be substantially centered on the fourth data element.